DESIGN AND IMPLEMENTATION OF A CMOS SENSOR BASED VIDEO CAMERA INCORPORATING A COMBINED AWB/AEC MODULE

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ABSTRACT

This paper presents a design and hardware implementation of a CMOS sensor based video camera incorporating a module, which combines the functions of automatic white balancing (AWB) and automatic exposure control (AEC). The functionality is achieved using dynamic control of sensor registers using I2C sensor interface. The image data processing is performed using a field programmable gate array (FPGA). The combined AWB/AEC module can be implemented using a gate count of 10k. The results indicate that the implemented video camera produce desired functionality with good reaction time.

1. INTRODUCTION

Complementary Metal-Oxide Semiconductor (CMOS) imaging technology is emerging as an alternative solid-state imaging technology to charge coupled device (CCD) [1]. The main advantages of CMOS over CCD are low power consumption, low cost due to compatible manufacturing process with standard CMOS technology, and easy integration with other CMOS signal processing modules. Therefore, a possibility exists for combining low-level automatic sensor control functionality to be embedded with CMOS image sensors for one-chip solutions.

The research and implementation efforts are therefore directed towards developing simple but effective algorithms that can be implemented on hardware, consuming small area on silicon and requiring a small net gate count.

Automatic exposure control (AEC) and automatic white balancing (AWB) functionalities have now become standard features of most digital still and video cameras. It is envisaged that in the near future, these functionalities can become embedded within the CMOS image sensors. At present, most commercially available CMOS sensors provided user configuration of color channel gain, integration time, frame rate, capture mode etc. by simply setting internal configuration registers provided on-chip. Such flexible and easy control of image capture using CMOS sensors provide opportunities to develop algorithms that can be used for automatic configuration of registers.

Figure 1 shows the FPGA based programmable camera module used for implementation of the AWB/AEC module.

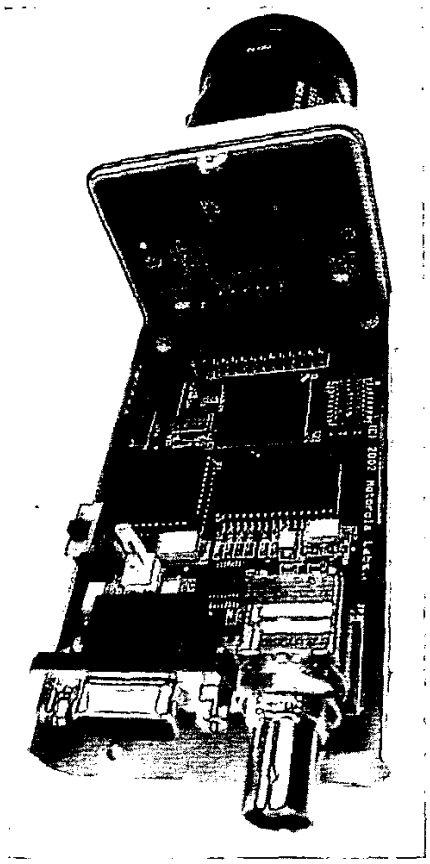

Figure 1: FPGA based Programmable camera module

2. CMOS SENSOR INTERFACE

The CMOS sensor used in this implementation was the Motorola MCM20014 1/3" Color VGA Digital Image Sensor with Bayer-RGB color filter array. Figure 2 shows the color sensor mounted on the designed PCB.

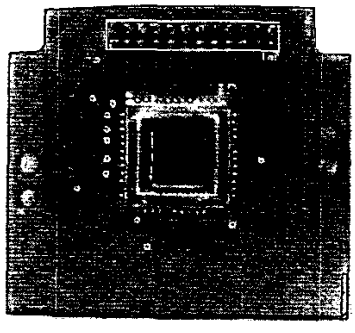

Figure 2: CMOS sensor board.

2.1 Sensor Control Registers

The relevant sensor registers for the implementation of the combined AWB/AEC module are shown in Table 1 [2].

Hex Address	Register Function	Default Value (REG)
01h	Red Gain	02h
02h	Blue Gain	02h
4Eh	Integration Time (ISB)	02h
4Fh	Integration Time (LSB)	0Ch
50h	Virtual Frame Row Depth (MSB)	02h
51h	Virtual Frame Row Depth (LSB)	0Ch

Table 1: Relevant Sensor Registers

It should be noted that the maximum integration time is limited by the virtual frame depth rows (VFDR). Therefore, VFDR should be increased together with integration time, resulting in lower frame rates at low lighting conditions.

2.2 I2C interface

A compact I2C data transfer [3] module was developed for control of the sensor configuration registers. The module is constructed to handle both read and write conditions, however since all register values are saved internally in the FPGA, only write mode is utilized. The module is subdivided into three modules; namely Clock_control, I2C_core, and I2C_control. The maximum transfer rate for I2C data transfer to MCM20014 sensor is 100kHz. The core starts by sending a device call and gets an acknowledgment back from the sensor, and then the address and data are transferred over the two bi-directional serial wires. Full description for writing one byte can be found in Figure 3. Gate count for the I2C module is 1.5k gates. The I2C_control module controls all changes to the sensor, including all control registers for the combined AWB/AEC module.

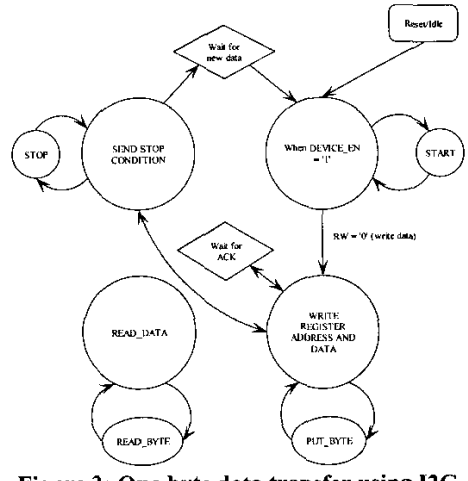

Figure 3: One byte data transfer using I2C.

3. COMBINED AWB/AEC MODULE

Automatic white balancing is based on "Gray World" model [4] [5], which means that the average of C_r and the average of C_b (chromaticity channels) should be zero. Thus, amplification in RGB channels should be adjusted until C_r and C_b are close to 0. It is a simple approach, but it introduces significant color distortions if a colored object occupies a majority in the scene and therefore "Gray World" model is not applicable. Introducing constraints can solve this problem. Since all natural illuminants are described by color temperature, light source can only changes from light blue to light red. The area covered by the natural sources is shown in Figure 4.

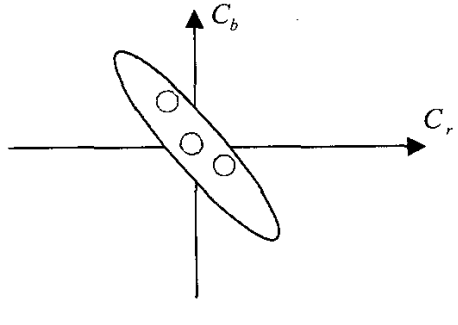

Figure 4: AWB C_r and C_b channel constraint.

This means that only R and B channels need to be controlled. Moreover, this control should be limited to stay within the area. This can be mapped into amplification of R and B channels, as shown in figure 5.

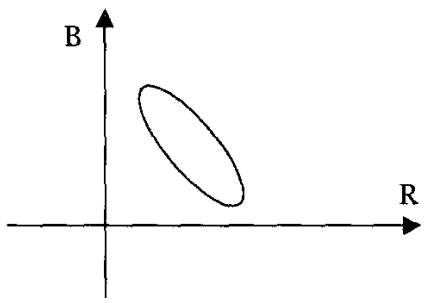

Figure 5: AWB R and B channel gain constraint.

Registers 01h and 02h of the DVGA sensor need to be controlled through I2C bus. Actual gain in the channel depends on the value REG (refer to Table 1) written in the corresponding register,

$$Amplification = 0.88 + 0.06*REG \quad (1)$$

Set to the default value for G_r and G_b channels are 06h and is not dynamically changed. The two channels are constrained:

$$3h > REG_b > 1Fh \quad (2)$$
$$0 > REG_r > 16h \quad (3)$$
$$0Ch > (REG_b + REG_r) > 1Fh \quad (4)$$

These constraints approximate the area shown in Figure 5. The algorithm is described below:

- Send default REG_b, REG_r, REG_{gr} and REG_{gb} to DVGA registers.
- **Label:** Produce R_{ave}, G_{ave}, and B_{ave} for window of interest (WOI).
- Produce C_b average = B_{ave} - G_{ave} and C_r average = R_{ave} - G_{ave}
- Check if the optimal white balance point is achieved (actually passed). An optimization criterion is min {C_b average, C_r average} < 3.
- If optimization is reached for R or B then "stop" the corresponding channel. If both are stopped then "sleep"
- Check if the process should be "wake up", by comparing average C_b and C_r against the old values produced just before "sleep"
- If B channel is not stopped then continue optimization with the constraints. If the average C_b is positive, REG_b is decremented by 1, otherwise incremented by 1. Send new REG_b to the sensor.
- If R channel is not stopped then continue optimization with the constraints. If the average C_r is positive, REG_r is decremented by 1, otherwise incremented by 1.Send new REG_r to the sensor.
- Loop to **Label.**

The G_{ave} value is computed for AWB. Since Green represents a large portion of the luminance, G_{ave} is used as the mean luminance to implement the AEC algorithm in the normal mode. For normal mode, the expected mean value for G channel is set to 127. The absolute difference between G_{ave} and 127 is used to compute the step size of integration time increase or decrease.

$$\text{Step size} = |G_{ave} - 127| / 2 \quad (4)$$

Since G_{ave} can vary between 0 and 255, the maximum step size will be 64. Therefore, the minimum integration time is set to 64 to avoid instability that can be caused by integration time becoming smaller than the step size.
The step size is added or subtracted from the current integration time depending on whether G_{ave} is smaller or larger than 127. In the NTSC video mode, the current implementation supports frame rates of 30fps, 15fps and 7.5fps. At 7.5fps, the virtual frame depth can be set to 2091 (hex values of two 8-bit registers). Therefore, the maximum integration time that is allowed is capped at 2091. In PAL mode (i.e. 25fps, 12.5fps, 6.25fps) it is possible to set the virtual frame depth to 2499. Therefore, it is possible in this mode to further increase the integration time to 2499. However, to keep the modifications to a minimum when switching from NTSC to PAL and vice versa, the maximum integration time is fixed at 2091.

4. RESULTS AND DISCUSSION

The algorithms were implemented on a Xilinx Virtex II FPGA platform. Separate experiments were conducted for characterizing the camera in terms of AWB and AEC performance. The relevant register values were accessed using an RS-232 interface implemented on the camera module.

For AWB performance testing, different color temperatures were used such as incandescent (2500K), halogen (3000K) and florescent (4000K) lighting as well as bright sunshine with clear sky (6000K) [6]. The resultant gains for red and blue channels are plotted against the color temperature, as shown in Figure 6. It can be clearly seen that at lower color temperatures (i.e.

reddish luminance), the blue channel gain increases while red gain is decreased to compensate for color imbalance (as shown in Figure 7). As expected, the color gains of the channels are reversed at higher color temperatures. As a result, and according to the gray-world assumption, the mean values for the R, G and B channels are equalized after white balancing. A color imbalance of 20.52% at incandescent lighting can be reduced to only 3.54% using the implemented algorithm. Since the constraints are imposed on the R and B register space, when a colored object occupies most of the field of view, gray world assumption is overridden to avoid loss of color saturation.

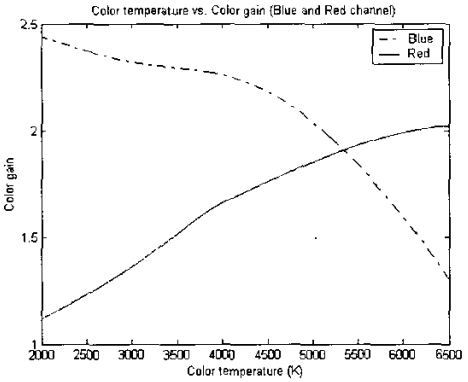

Figure 6: Color temperature vs. Red and Blue color gain

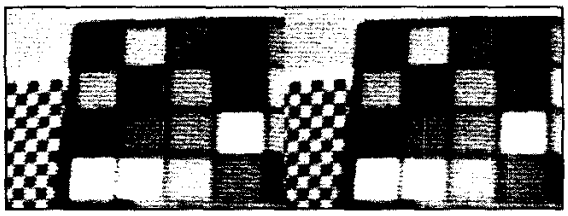

Figure 7: Left, with AEC and AWB, right without AWB, with AEC (250 LUX, Incandescent lighting).

AEC performance testing was conducted using a variable incandescent illuminant. The illumination was measured using a TENMA 72-6693 Digital Light Meter. In order to record the response times, illumination was instantly changed from 0 Lux to a pre-defined level (e.g. 100, 200, 400 and 1000 Lux). After steady state is reached, illuminant was withdrawn resulting in 0 Lux level. The response curves are shown in Figure 8. It can be seen that typical response is 1-3 seconds for luminance increase, whereas for luminance decrease it is longer (1-4 seconds). The longer response time for luminance decrease is due to the necessity of reducing the frame rate. The frame rate was reduced from 30fps, to 15fps or 7.5fps depending on the luminance level. A comparison of image quality with and without AEC is shown in Figure 9, with AWB enabled.

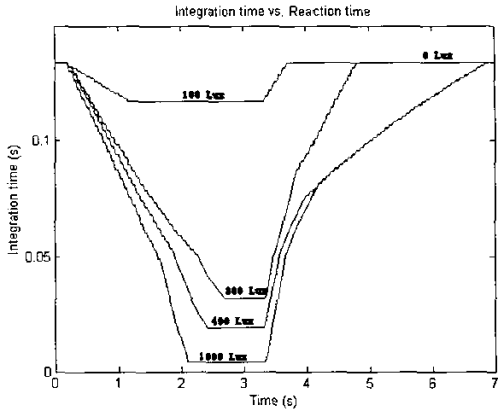

Figure 8: Integration time vs. Reaction time

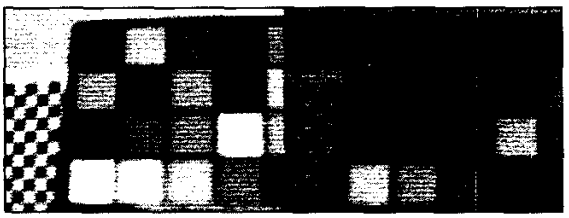

Figure 9: Left, with AEC and AWB, right without AEC, with AWB (250 LUX, Incandescent lighting).

5. CONCLUSION

A combined AWB/AEC module was developed and implemented on an FPGA, using a gate count of 10K including memory buffers. Both the color channel gains and integration time were dynamically controlled using configurable registers provided on the CMOS sensor. The functionality of AWB and AEC were measured separately. The results indicate that the implemented module provides good accuracy and response times.

6. REFERENCES

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