A 96 × 64 INTELLIGENT DIGITAL PIXEL ARRAY WITH EXTENDED BINARY STOCHASTIC ARITHMETIC

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ABSTRACT

A chip architecture that integrates an optical sensor and a pixel level processing element based on binary stochastic arithmetic is proposed. The optical sensor is formed by an array of fully connected pixels, and each pixel contains a sensing element and a Pulse Frequency Modulator (PFM) converting the incident light to bit streams of identical pulses. The processing element is based on binary stochastic arithmetic to perform signal processing operations on the focal plane VLSI circuit. A 96 × 64 CMOS image sensor is fabricated using $0.5\mu m$ CMOS technology and achieves $29 \times 29\mu m$ pixel size at 15% fill factor.

1. INTRODUCTION

Pixel level processing and pixel level ADC are at the centre of Smart Integration Solution system research. The introduction of ADC at the pixel level will permit all of the post pixel signal processing to be performed digitally, thereby, significantly reducing the amount of analog circuitry required.

The addition of pixel level memory allows imaging data to be stored locally and accessed in a manner similar to standard DRAM memory. Therefore, the trend towards higher transistor densities with each successive semiconductor technology generation makes it highly probable that image sensors using pixel level ADC will be widespread in the near future. However, the operation voltage decreases accompanied with such a deep sub-micron process, and it may directly affect the signal quality and thus deteriorate a signal-to-noise-ratio (SNR). In addition, the area of a photodiode decreases as the process rule becomes fine, and consequently the signal capacity in the photodiode decreases, which also causes to degrade the SNR.

Thus, the big challenge today is to develop robust smart image sensor architecture that can deal with low operation voltage and reduced photodiode area.

Pulse coded arithmetic and stochastic neural arithmetic are biologically inspired networks that have been extensively studied and have been used for characters recognition and pattern recognition tasks [1]. However, most of the work on stochastic arithmetic is limited to software implementation and simulation and very little work was reported on the hardware implementation.

In this paper we present a robust smart image sensor architecture with fully connected pixel level stochastic arithmetic processor. The sensor is capable of image capture as well as image computation. In Section 2 of this paper we will present the pixel architecture, we will demonstrate that Pulse Frequency Modulation (PFM) is well compatible with digital logic circuits and robust against noise. It is essentially digital circuits, thus deep sub-micron technology is applicable to it and the operation voltage hardly affects the SNR. In Section 3, we present the concept of using stochastic arithmetic on the focal plane VLSI image sensor circuit, simulation results of the MATLAB model of the sensor performing image capture and contrast enhancement is presented. In the next Section we describe the image sensor implementation and the characteristic of the testing prototype. Finally in Section 5 we present the conclusion.

2. PIXEL LEVEL CONVERSION

The main advantage of our pixel level conversion method is that the circuit is essentially digital well suitable for deep-micron technology. Another advantage, the output is pulse train which means the operation voltage hardly affects the SNR. As illustrated in Figure. 1, the pixel architecture consists of a sensing element(n^+psub photodiode PD) a reset circuit, and a clocked comparator.

2.1. Pixel Functionality

The photodiode acts as a variable current source controlled by the input light intensity and is charged through the reset transistor M1. The gate of M1 is switched by the feedback of the inverted comparator output. The analog value of the light intensity is then consequently converted into a pulse train coded signal. Figure. 2 demonstrates SPICE simulation of the functional operation of the pixel. The volt-

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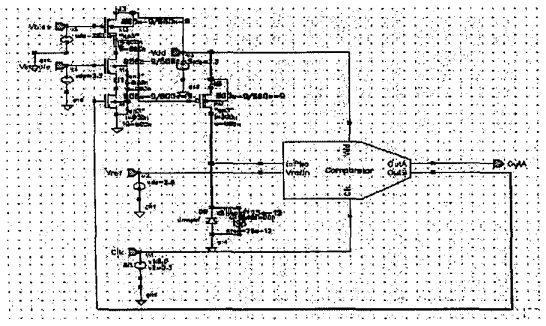

Figure 1: Image capture pixel architecture.

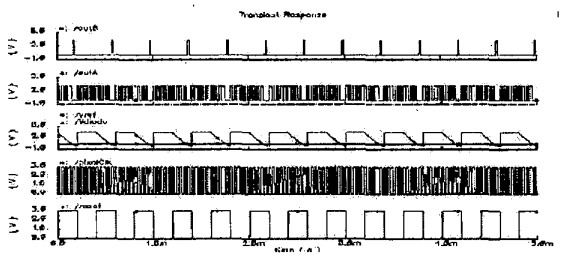

Figure 2: Pixel functionality SPICE simulation.

age V_D across the node of the photodiode is compared to a programmable clocked comparator reference voltage V_{ref}, as light illuminates PD, V_D gradually drops from the bias voltage of the reset transistor M1 by the photocurrent and finally reaches V_{ref}, this operation will switch the output of the comparator and the feedback circuit will reset the photodiode node to V_{dd}. In this case, if I_{ph} and C_D represent the photocurrent and the photodiode internall capacitor, respectively, we can express the oscillating frequency f as:

$$f \approx \frac{1}{T_D} = \frac{I_{ph}}{(V_r - V_{ref}) \times C_D} \tag{1}$$

where T_D represents the integration time, it describes the time needed for the photodiode to discharge from V_r (the bias voltage of the reset transistor) to V_{ref}. From Eq. (1) it can be concluded that the oscillation frequency f, or the firing rate, increases if the input light intensity becomes large and the size of the photodiode becomes small. This therefore makes this type of oscillating pixels suitable for low voltage operations and deep sub-micron technology. A large well capacity is no longer necessary, this is mainly because of the reuse of the well capacity during integration due to these oscillations.

In order to achieve a programmable high dynamic range and adaptation to different lighting conditions, we developed a compact programmable counter and windowing readout strategy to achieve high frame rate imaging capability. It is possible to control the counter to adapt the dynamic range to different lighting condition or to extend the dynamic range to values over 100 db. This can be easily demonstrated by the following equations:

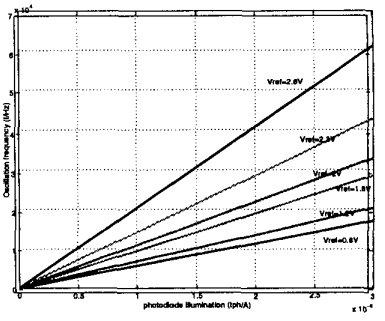

Figure 3: Photodiode linear characteristic.

$$N_{pulse} = \frac{T_{count}}{T_D} = \frac{T_{count} \times I_{ph}}{(V_r - V_{ref}) \times C_D} \tag{2}$$

then the counting period can be expressed as follow:

$$T_{count} = N_{pulse} \times \frac{(V_r - V_{ref})}{I_{phmax}} \times C_D \tag{3}$$

in our case $N_{pulse} = 2^n$. By controlling T_{count} we can optimize the dynamic range for different lighting conditions as well as the conversion speed. The minimum detection limit can be determined by the dark current as well as the leak current of the reset transistor, the minimum frequency can be given by:

$$f_{min} = \frac{I_{leakage}}{(V_r - V_{ref}) \times C_D} \tag{4}$$

If we assume that the leakage current of the photodiode is few fA, the minimum frequency can be estimated to $10Hz$. Thus, by exploring Eq. 4, we can conclude that the dynamic range can be expanded by adaptively changing the voltage. However, in order to take full advantage of the pixel architecture, a sensor callibrating faze is very important to generate the external signals needed to achieve the expected dynamic range. Figure. 3 illustrates the linearity of the photodiode.

2.2. Clocked comparator

The heart of the bit stream conversion at the pixel level is a dynamic latch type comparator. This type of circuits are

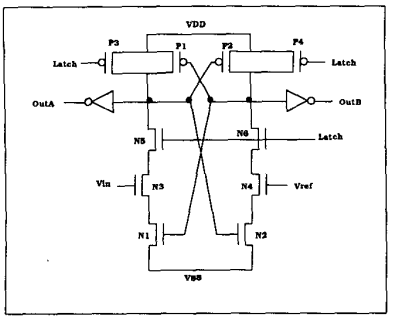

Figure 4: Clocked comparator.

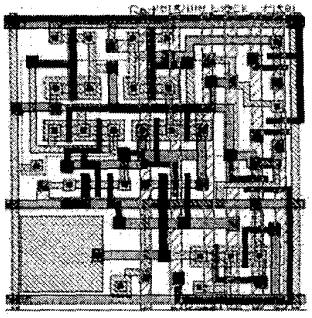

Figure 5: Pixel layout.

commonly used in DRAM's and SRAM's as a sense amplifier. When it's applied as a comparator, a dramatic reduction in the power dissipation can be expected. Figure. 4 shows the schematic of the comparator used. When the clock pulse is low, the supply current is cut off and the outputs are connected to V_{dd} through switches $P3$ and $P4$, the input transistors $N3$ and $N4$ are in triode mode. When a signal is applied to these two MOS gates differentially and the clock pulse goes high, the output of the stronger side $N3$ and $N4$ is pulled down more strongly than the other side. This will cause the latch to flip to one of the two stable states.

3. PIXEL LEVEL STOCHASTIC ARITHMETIC

The main objective of this work is the development of smart imaging devices with programmable processing capability in this section we describe the principle behind pixel level stochastic arithmetic.

Given a set of analog (pixel input) inputs, they are stochastically converted using the frequency modulator, then processed, and finally recovered from the stochastic pulse stream as a digital value. The main advantage of the stochastic processing system is the possibility of doing pseudo-analog functions working with the value of the pulse stream, but with a digital implementation. It is well known that a probability cannot be exactly measured but only estimated as the relative frequency of "high" levels in a long enough sequence. As a consequence, the stochastic computing introduces errors in the form of variance when we attempt to estimate the number from the sequence.
If $Z = \sum_i \frac{X_i}{n}$ the relative frequency of $1s$ in n pulse sequence $X_1, X_2....X_n$. Expectation value and variance of Z are given respectively by

$$E[Z] = \sum_{1}^{n} \frac{\mu_i}{n} \tag{5}$$

$$Var[Z] = E[Z - E[Z]]^2 = \frac{1}{n^2} \sum_i \sigma^2 \tag{6}$$

Where μ_i and σ_i are the mean value and the typical deviation respectively for each X_i.

From figure. 2 the pixel functionality can be described as detection of presence or absence of a signal on each clock cycle. This result on streams of Bernoulli probability $P_i = p(x_i = 1)$ on each clock cycle. As expressed in Eq. 7, P_i is determined by the relative magnitude of the expected signal to the V_{ref} of the comparator, and by the variance of the zero mean gaussian noise on the signal.

$$P_i = \frac{1}{\sqrt{2\pi\sigma_N^2}} \int_{V_{ref}}^{\infty} e^{\frac{(\nu - V_m)^2}{2\sigma_N^2}} d\nu \tag{7}$$

The integration imager communications involve only serial bit streams of identical pulses. The main advantage of stochastic computing is the similarity between Boolean algebra and statistical algebra. When a stochastic signal $Sgn(t)$ is multiplied by weighting coefficient $0 \leq w \leq 1$, the multiplication can be achieved by using a simple AND gate. Addition of two stochastic signals $Sgn1(t)$ and $Sgn2(t)$ can be obtained by combining them in an OR gate [2]. Each pixel involve an AND gate to perform the weighted multiplication. None of these operations affects the SNR of the resulting signal [2]. It is possible by using a suitable distributed architecture at the pixel level and with minimum hardware to perform a weighted sum which is the standard task in image processing, such as low-pass filtering, removal isolated nonzero pixels, or edge detection.

In order to prove the concept of stochastic arithmetic we built a model of the sensor in Matlab (Simulink) to emulate the behavior of the intelligent CMOS digital pixel. The main objective of the model is to generate hyper-spectral test images from synthetic scenes with the introduction of

Figure 6: Simulation of the MATLAB model of the sensor. SICNN using pulse stochastic arithmetic

the physics-based model of the optical and CMOS solid-state elements of the imager. The stochastic arithmetic operations were based on the SICNN contrast enhancement algorithm we introduced in [3]. Equation. 8 illustrates the mathematical equation of SICNN.

$$X_{ij} = \frac{I_{ij}}{a_{ij} + \sum_{k,l \in N_r(C)} w_{ij} I_{kl}} \tag{8}$$

Where x_{ij} represents the SICNN output pixel, I_{ij} is the input pixel, $a_{ij} (= 1)$ is a constant; the term $\sum_{k,l \in N_r(C)} w_{ij} I_{kl}$ represents a convolution operation or the weighted sum. For simplicity reasons the convolution mask used is,

$$W = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 1 \end{bmatrix}$$

Figure. 6 shows the simulation results of the sensor model.

4. VLSI PROTOTYPE

In this design a 96×64 pixel array with counter length of 8bits has been implemented. The chosen configuration is sufficient for a feasibility demonstration. The increase of the precision of the frequency measurement by adding more counters (One counter for each 3×3 pixels) stages in the design is straightforward for technologies $< 0.5\mu m$. Figure. 7 shows the prototype imager fabricated in $0.5\mu m$, 1 poly/4 metals CMOS standard technology. The pixel layout is shown in Figure. 5, it occupies an area of $29 \times 29\mu m^2$ with a fill factor of 15%. The average power consumption per pixel at a frequency of $150khz$ is $78\mu W$. The test chip will allow us to test the expected dynamic range and also evaluate simple image processing operations based on stochastic arithmetic.

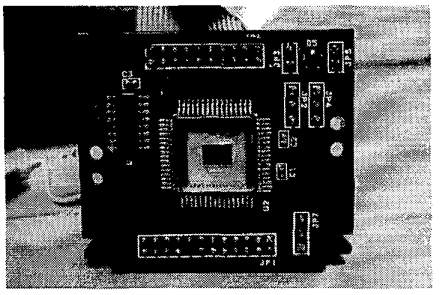

Figure 7: The CMOS imager prototype.

5. SUMMARY AND FUTURE WORK

In this paper the authors introduced a robust pixel architecture suitable for deep submicron technology demonstrating an adaptive wide dynamic range exceeding 100 db without affecting the SNR. We demonstrated that it is possible to take advantage of the concept of stochastic arithmetic to implement complex image processing algorithms. To the best of our knowledge this paper is the first in demonstrating a pixel level stochastic arithmetic. As mentioned earlier the main advantage of the stochastic processing system is the possibility of doing pseudo-analog functions using the values of the pulse stream, but with digital implementation.

More issues related to deep sub micron technology need to be addressed in the future. We predict that digital pixel architecture (DPS) technology will flourish with the availability of photodectors characterization data from foundaries, and the development of new sensors introducing pixel level stochastic arithmetic, this situation will lead to the establishment of an advanced technology taking over the dominance of CCDs.

6. REFERENCES

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